REMARKS

Review and reconsideration on the merits are requested

The Prior Art

High-Quality Growth of AlN Epitaxial Layer by Plasma-Assisted Molecular-Beam Epitaxy, Jeganathan et al. (Jeganathan); U.S. 5,810,925 Tadatomo et al. (Tadatomo); U.S. 6,040,588 Koide et al. (Koide '588); U.S. 6,420,733 Koide (Koide '733); U.S. 6,407,409 Cho et al. (Cho).

The Rejections

All rejections are obviousness rejections.

All claims, claims 1-2 and 8, are rejected under 35 U.S.C. § 103(a) as being obvious over Jeganathan in view of Tadatomo or Koide '588 or Koide '733 or Cho.

The above rejections are respectfully traversed.

Traversal

In contrast to the present invention, Jeganathan teaches the growth and characterization of high-quality h-AIN epitaxial layers on a basal c-plane sapphire substrate by plasma-assisted molecular-beam epitaxy (MBE) to produce AIN films suitable for an insulator for fabricating devices with insulated gates such as a metal-insulator-semiconductor field effect transistor (MISFET) and an insulated gate filed effect transistor (IGFET) (see Abstract; page L-28, left column, lines 15-25, of Jeganathan). Jeganathan fails to teach or suggest a self-supported nitride

semiconductor substrate as in amended claim 1 of the present application for the following reasons.

To explain the features of the Jeganathan's AIN films, Applicants site Document 1 reporting MISFET in an article entitle "Performance of AIN/GaN Heterostructure Metal Insulator Semiconductor Field Effect Transistor Based on Two-dimensional Monte Carlo Simulation" by Syunji Imanaga and Hiroji Kawai, copy attached. (Jpn. J. Appln. Phys. Vol. 39 (2000), Pt. 1, No. 4A, pp. 1678-1682)

Document 1 teaches one example of MISFET in Fig. 1 at page 1678 thereof, where AIN is formed on a different type of semiconductor such as P-GaN, on which a Gate electrode is formed.

Applicants now explain MISFET.

A MOSFET corresponding to conventional technology of a MISFET has used SiO_2 as a gate insulation film thereof. However, the MOSFET has a bottleneck in increasing device properties such that the interface state density of a MOSFET is large, so that an electron is trapped in the interface state on the interface between a gate insulation film using SiO_2 as a insulator and a semiconductor layer positioned as an underlayer threof, and accofdingly, the effective carrier density of the inversion layer decreases (decrease in apparent effective electron mobility), thereby causing an increase in channel resistance of the MOSFET.

The problem with a MOSFET as mentioned above has been solved by a MISFET using AIN as the gate insulation film thereof in place of SiO_2, aiming at realizing high effective electron mobility by controlling the interface state density to a minimum (please refer to page L-

28, left column, lines 23-25, of Jeganathan). Thus, it is necessary to establish the growth of a high quality AlN crystal having high insulation characteristics as a precondition for achieving the goal above mentioned which Jeganathan discusses.

The necessary thickness of the gate insulation fillm of a MISFET is generally thin, i.e., in a range of several nm to several hundred nm, far different from the thickness of 50 μm or more for the self-supported nitride semiconductor substrate of the present invention.

Thus, Jeganathan is wholly different from the present invention in technology, and, accordingly, the technical ides is wholly different.

Additionally, Jeganathan uses an MBE method for the growth of AlN films on a sapphire substrate, which is different from various methods used in the present invention such as a sublimination method, a metal-organic vapor phase epitaxy (MOVPE) method, a hydride vapor-phase epitaxy (HPVE) method, a liquid-phase epitaxy method, an epitaxial lateral overgrowth (ELO) method, or a combination thereof (see page 5, lines 19-24, of the specification).

The MBE method allows crystal growth at an atomic layer level under ultra-high vacuum conditions, thereby making it possible to advantageously carry out crystal growth at high purity but disadvantageously at a very low speed. Accordingly, those skilled in the art use the MBE method only in producing ultra-thin semiconductor films as general common good sense.

Thus, Jeganathan doe not teach or suggest the supported nitride semiconductor substrate at least having a diameter of 10 mm or more, and a thickness of 50 μm or more.

Therefore, one skilled in the art referring to Jeganathan would not be motivated to reach the invention of amended claim 1, and, accordingly, amended claim 1 is not obvious over Jeganathan.

With respect to Tadatomo, although the Examiner states in at page 3, lines 14-15, of the Action that:

> "Tadatomo discloses GaN grown on a sapphire substrate to a thickness of not less than 80 μm and discloses this thickness as sufficiently thick enough to permit its use as a substrate. Tadatomo discloses the thick nitride material is used for semiconductor light emitting elements,"

it is clear that the teaching of Tadatomo does not remedy the defects of Jeganathan in not teaching a self-supported nitride semiconductor substrate having a diameter of 10 mm or more and a thickness of 50 μm or more as claimed.

Therefore, one skilled in the art referring to Jeganathan would not be motivated at the time the present invention was made to incorporate the teaching of Tadatomo into the teaching of Jeganathan to reach the present invention as claimed in the present application, and, accordingly, amended claim 1 is not obvious over Jeganathan in view of Tadatomo.

Applicants rely upon their arguments for claim 1 regarding claims 2 and 8.

With respect to the remaining rejections, Applicants submit that the teaching of Koide '588, Koide '733 and Cho do not remedy the defects of Jeganathan which fails to teach a self-supported nitride semiconductor substrate have a diameter of 10 mm or more and a thickness of 50 μm or more as now claimed.

Withdrawal of all rejections and allowance is requested.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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